We claim:

1. A method of cooling a semiconductor chip, comprising:

providing a number of electrical devices on a semiconductor layer of the semiconductor chip;

integrally forming a substantially planar heat conducting layer with the semiconductor layer, wherein the heat conducting layer is compatible with semiconductor processing techniques, the heat conducting layer being adjacent to the number of electrical devices, the heat conducting layer having a higher thermal conductivity than the semiconductor layer;

conducting heat generated by the number of electrical devices into the heat conducting layer; and

transmitting the heat generated by the number of electrical devices through the heat conducting layer from a first region having a first temperature to a second region having a second temperature that is lower than the first region.

2. The method of claim 1, wherein providing a number of electrical devices includes providing a number of transistors.

3. The method of claim 1, wherein coupling a heat conducting layer to the semiconductor layer comprises coupling a carbon containing layer to the semiconductor layer.

4. The method of claim 3 wherein coupling a carbon containing layer to the semiconductor layer comprises coupling a diamond containing layer to the semiconductor layer.

5. The method of claim 1, further comprising transmitting heat from the heat conducting layer to a location remote from the semiconductor processor chip.

6. A method of cooling a semiconductor chip formed from a semiconducting material, comprising:

integrally coupling a substantially planar heat conducting layer to the semiconductor chip, wherein the heat conducting layer is compatible with semiconductor processing techniques, the heat conducting layer having a higher thermal conductivity than the semiconducting material;

conducting heat from the semiconductor chip into the heat conducting layer; and

transmitting the heat through the heat conducting layer from a first region having a first temperature to a second region having a second temperature that is lower than the first temperature.

7. The method of claim 6, wherein coupling a substantially planar heat conducting layer to the semiconductor chip includes coupling a carbon containing layer to the semiconductor chip.

8. The method of claim 7, wherein coupling a carbon containing layer to the semiconductor chip includes coupling a diamond containing layer to the semiconductor chip.

9. The method of claim 6, further comprising transmitting heat from the heat conducting layer to a location remote from the semiconductor chip.

10. A method of cooling a semiconductor chip, comprising:

integrally forming a diamond containing layer adjacent to a number of electrical devices on a semiconductor layer;

conducting heat generated by at least a portion of the number of electrical devices in a first area into the heat conducting layer; and

spreading the heat generated by the electrical devices in the first area through the heat conducting layer to a larger second area wherein heat per unit area is reduced.

11. The method of claim 10, wherein integrally forming a diamond containing layer adjacent to a number of electrical devices includes integrally forming a diamond containing layer adjacent to a number of transistors.

12. The method of claim 10, further comprising transmitting heat from the diamond containing layer to a location remote from the semiconductor processor chip.

13. The method of claim 10, wherein integrally forming a diamond containing layer adjacent to a number of electrical devices includes integrally forming a diamond containing layer on an active side of the semiconductor processor chip.

14. The method of claim 10, wherein integrally forming a diamond containing layer adjacent to a number of electrical devices includes integrally forming a diamond containing layer on a back side of the semiconductor processor chip.

15. The method of claim 10, wherein integrally forming a diamond containing layer adjacent to a number of electrical devices includes integrally forming a diamond containing layer between an active side and a backside of the semiconductor processor chip.

16. A method of manufacturing a semiconductor chip, comprising:

fabricating a semiconductor layer;

forming a number of electrical devices on the semiconductor layer;

electrically connecting the number of electrical devices; and

integrally forming a substantially planar heat conducting layer operatively connected to the semiconductor layer, wherein the heat conducting layer is compatible with semiconductor processing techniques, the heat conducting layer being adjacent to the number of electrical devices, the heat conducting layer having a higher thermal conductivity than the semiconductor layer.

17. The method of claim 16, wherein fabricating a semiconductor layer includes fabricating a silicon substrate.

18. The method of claim 16, wherein forming a substantially planar heat conducting layer includes forming a carbon containing layer.

19. The method of claim 18, wherein forming a carbon containing layer includes forming a diamond containing layer.

20. The method of claim 19, wherein forming a diamond containing layer includes chemical vapor deposition (CVD) depositing a diamond layer.

21. A method of manufacturing a semiconductor chip, comprising:
forming a number of transistors on a semiconductor layer;
electrically connecting the number of transistors; and
integrally forming a substantially planar diamond containing layer operatively connected to the semiconductor layer, and adjacent to the number of transistors.

22. The method of claim 21, wherein forming a number of transistors on a semiconductor layer includes forming a number of transistors on a silicon substrate.

23. The method of claim 21, wherein integrally forming a substantially planar diamond containing layer operatively connected to the semiconductor layer, and adjacent to the number of transistors includes integrally forming a substantially planar diamond containing layer on an active side of the semiconductor chip.

24. The method of claim 21, wherein integrally forming a substantially planar diamond containing layer operatively connected to the semiconductor layer, and

adjacent to the number of transistors includes integrally forming a substantially planar diamond containing layer on a back side of the semiconductor chip.

25. The method of claim 21, wherein integrally forming a substantially planar diamond containing layer operatively connected to the semiconductor layer, and adjacent to the number of transistors includes integrally forming a substantially planar diamond containing layer between an active side and a back side of the semiconductor chip.

26. A method of forming an electronic system, comprising:

forming a processor chip, including:

forming a number of transistors on a semiconductor layer;

electrically connecting the number of transistors;

integrally forming a substantially planar diamond containing layer operatively connected to the semiconductor layer, and adjacent to the number of transistors; and

coupling the processor chip to a random access memory.

27. The method of claim 26, wherein forming a substantially planar diamond containing layer includes chemical vapor deposition (CVD) depositing a diamond layer.